REMARKS

Claim Status

Claims 1, 6-8, 23-28, and 33-35 are pending.

Claims 1, 6-8, 23-28, and 33-35 stand rejected.

Claim Rejections under 35 U.S.C. §112, second paragraph

The Examiner rejected Claims 1, 6-8, 23-25, 27-28, and 33-35 under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to Claim 1, the Examiner stated that it is not clear whether the wafer used for testing the semiconductor tool includes the coating or not. In response, Claim 1 has been amended to recite "testing a semiconductor tool using the coated wafer".

Claim 6 depends from Claim 1 and is thus allowable for at least the reasons provided for Claim 1.

With respect to Claim 7, the Examiner stated that it is not clear that the testing surface contaminant adding properties tests scattering properties of a surface of the wafer or tests scattering properties of a surface of the coating and a surface of which coating is tested. In response, Claim 7 has been amended to recite "testing light scattering properties of a surface of the coating of the wafer".

Claim 8 depends from Claim 1 and is thus allowable for at least the reasons provided for Claim 1.

With respect to Claim 23, the Examiner stated that it is not clear where a polysilicon layer is provided. In response, Claim 23 has been amended to recite "wherein the providing a coating comprises: providing a polysilicon layer over the wafer".

With respect to Claim 24, the Examiner stated that it is not clear where a polysilicon layer is provided. In response, Claim 24 has been amended to recite "providing a polysilicon layer over a portion of the wafer where the coating was removed by grinding".

With respect to Claim 25, the Examiner stated that it is not clear whether contaminants are removed from a surface of the coating or replaced coating. In response, Claim 25 has been amended to recite "removing contaminants from a surface of the coating of the wafer used to test the semiconductor tool".

With respect to Claim 27, the Examiner stated that it is not clear where a polysilicon layer is provided. In response, Claim 27 has been amended to recite "providing a polysilicon layer over a portion of the wafer where the coating was removed by grinding".

Claim 28 depends from Claim 27 and is thus allowable for at least the reasons provided for Claim 27.

Claim 33 has been rejected but no basis for rejection is provided. Withdrawal of the rejection of Claim 33 under 35 U.S.C. §112, second paragraph is requested.

With respect to Claim 34, the Examiner stated that it is not clear that the testing surface contaminant adding properties comprises testing scattering properties of an uncoated surface of the wafer or testing scattering properties of a coated surface of the wafer. In response, Claim 34 has been amended to recite "testing surface contaminant adding properties comprises testing light scattering properties of a surface of the coating of the wafer".

Claim 35 has been rejected but no basis for rejection is provided. Withdrawal of the rejection of Claim 35 under 35 U.S.C. §112, second paragraph is requested.

Withdrawal of the rejections of Claims 1, 6-8, 23-25, 27-28, and 33-35 under 35 U.S.C. §112, second paragraph is requested.

Claim Rejections under 35 U.S.C. §102

Claims 1, 6, 8, 25, 26, 33, and 35 stand rejected under 35 U.S.C. §102(e) as being unpatentable over Rojhantalab et al. (U.S. Patent 6,761,625) (hereafter "Rojhantalab").

Claim 1 recites in pertinent part:

"providing a coating over a wafer ... replacing at least a portion of the coating of the wafer with a layer of coating".

Claim 26 recites in pertinent part:

"replacing at least a portion of a coating of a wafer with a layer of coating".

Rojhantalab discloses

"test wafer may be polished and re-used" (col. 1, lines 11-13) and "[b]efore polishing, the wafer has thickness D_1 . Polishing according to one embodiment of the present invention breaks the surface attachments or bonding between the particles and the wafer ... after polishing to remove the particles from the wafer surface, wafer 301 has a thickness D_2 which is not more than 500 Angstroms thinner than D_1 ." (Emphasis added) (col. 2, lines 54-56).

Accordingly, Rojhantalab discloses **removing** a portion of a test wafer and re-using a test wafer with a reduced thickness. Clearly, Rojhantalab does not teach "providing a coating over a wafer ... replacing at least a portion of the coating of the wafer with a layer of coating" of Claim 1 or "replacing at least a portion of a coating of a wafer with a layer of coating" of Claim 26.

Claims 6, 8, and 25 depend from Claim 1 and thus are allowable

for at least the same reason as pertains to Claim 1. Claims 33 and 35 depend from Claim 26 and thus are allowable for at least the same reason as pertains to Claim 26. Applicant requests withdrawal of the rejection of Claims 1, 6, 8, 25, 26, 33, and 35 under 35 U.S.C. §102(e).

Claim Rejections under 35 U.S.C. §103(a)

In an interview with the Examiner on March 22, 2006, the Examiner indicated that Claim 34 instead of Claim 37 should have been rejected under 35 U.S.C. §103(a). Accordingly, Claims 7 and 34 are rejected under 35 U.S.C. §103(a) as being unpatentable over Rojhantalab in view of Steigneier et al (U.S. Patent No. 4,526,468) (hereafter "Steigneier"). At page 7 of the Office Action, the Examiner admits that Rojhantalab does not teach "testing light scattering properties on the coated wafer including coating comprising at least one characteristic of a single crystal structure". At page 7 of the Office Action, the Examiner states that Steigneier teaches testing light scattering properties on the coated wafer comprising the single crystal structure to detect defect/contaminants of the coated wafer.

Steigneier does not cure the deficiencies of base Claims 1 and 26 stated earlier. Claims 7 and 34 depend from respective base Claims 1 and 26 and thus are allowable over the teachings and suggestions of Rojhantalab and Steigneier for at least the same reasons as stated with respect to Claims 1 and 26.

Final Remarks

The enclosed remarks are not intended to be an exhaustive enumeration of all distinctions between any cited references and the

PAGE 13

Application No. 10/718,102

claims. The distinctions identified and discussed are to illustrate at least one difference between the claims and the cited reference.

Applicant requests allowance of all pending Claims (namely, Claims 1, 6-8, 23-28, and 33-35).

If the Examiner has any questions concerning this application, please call the applicant's attorney at (212) 661-5488.

If there are any charges, please charge Deposit Account No. 50-0221.

Respectfully submitted,

Date: March 24, 2006

/Glen B. Choi/ Glen B. Choi

Reg. No. 43,546

ATTORNEY FOR APPLICANTS

Intel Corporation Mail Stop SC4-202 P.O. Box 5326 Santa Clara, CA 95056-5326 (212) 661-5488

CERTIFICATE OF TRANSMISSION

37 C.F.R. § 1.8(a)

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on March 24, 2006.

Name:

Glen B. Choi

Signature: _/Glen B. Choi/_